The effects of the ringing phenomenon in digital systems can be predicted and mathematically computed. They can be eliminated by choosing a suitable logic family for the system. Described here are some current methods of matching impedance levels which are incorporated in the design of integrated circuits

An Analysis of the Ringing Phenomenon in Digital Systems

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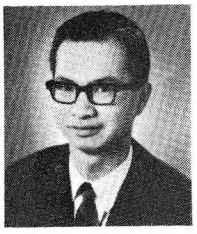
One of the most important factors to consider when designing an interconnection system for data processing equipment with high-speed digital ICs is the switching characteristics of these devices. Voltage switching between the two logic states—i.e., the transition between "0" and "1" and that between "1" and "0"—is chiefly affected by the impedance, the inductance, and the capacitance of the interconnecting cables, including those of the PC boards. It is also affected—to a very important degree—by the output impedance of the driver gates and the input impedance of the driven ones. At low frequencies these switching actions do not really cause noticeable disturbing effects on the total system itself. However, at high frequencies, especially with systems where digital ICs with relatively short transient response are used, overshoots as well as undershoots—and thus free energy—would create quite a few problems. This would necessitate a careful design of the power supply and the interconnection system. In some cases, because of noise and other disturbing influences, even a redesign of the whole system may be necessary.

It is certain that at high frequencies, where most digital systems are operating, one can no longer consider the connections between driver gates and driven ones as short circuits. Instead, they must be regarded as transmission lines with an impedance designated Z_0. In order to minimize the ringing problem and consequently to avoid a reduction of the system operating speed, and at the same time to guarantee a proper and reliable performance of the total system, efforts must be made to provide suitable terminations for these connections. A clamping effect by means of a diode between ground and the gate input was introduced as one of the solutions. This is, however, not sufficient. An improvement made to the gate output would provide a further substantial reduction of the ringing level.

This article provides a detailed analysis of the switching characteristics involved in the applications of high-speed ICs. Based on this analysis, one can predict the level of ringing, the spike current, and any matching requirement, and can, therefore, be in a position to decide clearly what must be done to avoid a deterioration in the system performance. In the second part of this article, the discussion covers the subject of ringing related particularly to a family of TTL ICs, commercially known as high level TTL.



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The Switching Function

As commonly known, there are two logic levels in digital systems: the true state or "1", and the false state or "0" (positive logic). The information signals being processed in such a system are in the form of square waves

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which can be mathematically described using the following equation:

$$u(t) = \frac{1}{2}(V_1 - V_0) + \frac{2}{\pi}(V_1 - V_0) \cdot (\sin \omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t + \ldots) \quad (1)$$

where V_1 and V_0 respectively represent the two voltage levels.

However, not all the signals appearing in a digital system are periodical. In order to simplify the analysis of this switching action and to give the result of this investigation a more realistic value, step functions have been chosen for this article. Further, since one can accept that both capacitance and inductance exist within an interconnection system, the following arrangement can be regarded as ideal for our analysis (Fig. 1). L, R, and C in this schematic represent the inductance, the capacitance, and the resistance. G, the conductance parallel to the capacitance, can conveniently be neglected. The following equation is applicable to the circuit as shown:

$$u(t) = u_L + u_R + u_C \quad (2)$$

where u is voltage.

If i(t) is the current, then

$$u(t) = L\frac{di}{dt} + iR + u_C$$

Replacing i(t) with its value at the time t, $C\frac{du}{dt}$, the following differential equation is obtained:

$$u(t) = LC\frac{d^2u}{dt} + CR\frac{du}{dt} + u_C \quad (3)$$

where u_C is the voltage appearing at time t across capacitor C.

This is a second degree differential equation which can be solved by considering the second part first; the solution will have the form

$$u(t) = A \cdot e^{at}$$

with $$\alpha_{1,2} = -\frac{R}{2L} \pm j\sqrt{\frac{R^2}{(2L)^2} - \frac{1}{LC}}$$

or, $$-\alpha_1 = \frac{1}{\tau} - j\omega_0$$

and $$-\alpha_2 = \frac{1}{\tau} + j\omega_0$$

where τ and ω_0 are the time delay and phase velocity, respectively, having the values

$$\tau = \frac{2L}{R};$$

$$\omega_0 = \sqrt{-\frac{1}{LC} + \left(\frac{R}{2L}\right)^2}$$

Therefore, the final solution to Eq. (3) would be

$$u(t) = A_1 \cdot e^{+\alpha_1 t} + A_2 \cdot e^{+\alpha_2 t} + B \quad (4)$$

The current equation will then be

$$i(t) = \alpha_1 \cdot A_1 \cdot Ce^{+\alpha_1 t} + \alpha_2 \cdot A_2 \cdot Ce^{+\alpha_2 t} + P \quad (5)$$

where A_1, A_2, B, and P are constants (defined and determined later in this article).

When switching from logic state "1" to logic state "0", the quiescent switching conditions which are important for the calculation of the overshoot caused by this voltage transient can be described as follows:

At the time t = 0,

$u(t) = V_1$, the logic "1" level,

$i(t) = I_1$, the leakage current;

after a certain period of time, at $t = t_1$, the ringing will be clamped and the voltage and current will be

$u(t) = V_0$, the logic "0" level,

$i(t) = I_0$, the current to ground of the gate input.

Applying these quiescent conditions to Eqs. (4) and (5), we obtain

$$V_1 = A_1 + A_2 + B \quad (6)$$

$$I_1 = A_1 \cdot \alpha_1 \cdot C + A_2 \cdot \alpha_2 \cdot C + P \quad (7)$$

$V_0 = B$ and

$I_0 = P$

Therefore, from Eq. (6)

$$A_2 = (V_1 - V_0) - A_1 \quad (8)$$

Replacing A_2 in Eq. (7) with the value given in Eq. (8):

$$I_1 = C\{A_1 \cdot \alpha_1 + \alpha_2(V_1 - V_0) - \alpha_2 \cdot A_1\} + I_0$$
$$= C\{A_1(\alpha_1 - \alpha_2) + \alpha_2(V_1 - V_0)\} + I_0$$

Therefore $$A_1 = \frac{\frac{1}{C}(I_1 - I_0) - \alpha_2(V_1 - V_0)}{\alpha_1 - \alpha_2} \quad (9)$$

and thus $$A_2 = \frac{\alpha_1(V_1 - V_0) - \frac{1}{C}(I_1 - I_0)}{\alpha_1 - \alpha_2} \quad (10)$$

The input current owing to the voltage transient becomes

$$i(t) = I_0 + C \cdot e^{-t/\tau} \cdot \left[\left\{\frac{\frac{1}{C} \cdot \alpha_1(I_1 - I_0) - \alpha_2\alpha_1(V_1 - V_0)}{\alpha_1 - \alpha_2}\right\}e^{j\omega_0 t} + \left\{\frac{\alpha_1\alpha_2(V_1 - V_0) - \alpha_2\frac{1}{C}(I_1 - I_0)}{\alpha_1 - \alpha_2}\right\}e^{-j\omega_0 t}\right]$$

or $$i(t) - I_0 = \frac{e^{-t/\tau}}{\alpha_1 - \alpha_2} \cdot [\{\alpha_1(I_1 - I_0) - \alpha_1\alpha_2C(V_1 - V_0)\}e^{j\omega_0 t} + \{\alpha_1\alpha_2C(V_1 - V_0) - \alpha_2(I_1 - I_0)\}e^{-j\omega_0 t}]$$

With $e^{-j\omega_0 t} = \cos \omega_0 t + j \sin \omega_0 t$

and $e^{j\omega_0 t} = \cos \omega_0 t - j \sin \omega_0 t$ (11)

$$i(t) - I_0 = \frac{e^{-t/\tau}}{\alpha_1 - \alpha_2} \cdot \{(I_1 - I_0)(\alpha_1 - \alpha_2)\cos \omega_0 t + j(\alpha_1 + \alpha_2)(I_1 - I_0)\sin \omega_0 t - 2j\alpha_1\alpha_2C(V_1 - V_0)\sin \omega_0 t\}$$

Further, the following expressions are applicable:

$$\alpha_1 - \alpha_2 = 2j\omega_0 \quad (12)$$

$$\alpha_1 + \alpha_2 = -\frac{R}{L} \quad (13)$$

$$\alpha_1 \cdot \alpha_2 = \frac{CR^2 - 2L}{2L^2C} \quad (14)$$

Therefore

$$i(t) - I_0 = e^{-t/\tau} \cdot \left\{ (I_1 - I_0) \cos \omega_0 t - \frac{R}{2\omega_0 L} (I_1 - I_0) \sin \omega_0 t + \frac{2L - R^2C}{2\omega_0 L^2} (V_1 - V_0), \sin \omega_0 t \right\} \quad (15)$$

To determine the amplitude of the first peak (overshoot), $t_1 = \pi/2\omega_0$ should be applied to Eq. (15):

$$I\left(\frac{\pi}{2\omega_0}\right) - I_0 = e^{-\frac{\pi R}{2L \cdot \omega_0}} \cdot \left\{ \frac{2L - R^2C}{2\omega_0 L^2} (V_1 - V_0) - \frac{R}{2\omega_0 L} (I_1 - I_0) \right\}$$

Using Eq. (15), one can also calculate the amplitude of the second peak (undershoot) if t is replaced with

$$t_2 = \frac{3\pi}{2\omega_0}$$

When switching from logic state "0" to logic state "1", the quiescent conditions applied will be as follows:

At the time t = 0,

$u(t) = V_0$, the logic "0" level,

$i(t) = I_0$, the current to ground of the gate input;

at the time $t = t_1$, when the switching action ends,

$u(t) = V_1$, the logic "1" level,

$i(t) = I_1$, the input leakage current.

Applying these conditions to Eqs. (4) and (5), we obtain

$$V_0 = A_1 + A_2 + B$$
$$I_0 = \alpha_1 A_1 C + \alpha_2 A_2 C + P$$
$$V_1 = B$$
$$I_1 = P$$

Therefore $A_2 = V_0 - V_1 - A_1$

and $$I_0 - I_1 = \alpha_1 C A_1 + \alpha_2 C (V_0 - V_1) - C\alpha_2 A_1$$
$$= C(\alpha_1 - \alpha_2) A_1 + C(V_0 - V_1)\alpha_2$$

From this equation one can obtain the value of the two constants, A_1 and A_2:

$$A_1 = \frac{\frac{1}{C}(I_0 - I_1) - \alpha_2 (V_0 - V_1)}{\alpha_1 - \alpha_2}$$

$$A_2 = \frac{\alpha_1 (V_0 - V_1) - \frac{1}{C}(I_0 - I_1)}{\alpha_1 - \alpha_2}$$

The current function will have the form of the following equation:

$$i(t) - I_1 = e^{-t/\tau} \left\{ (I_0 - I_1) \cos \omega_0 t - \frac{R}{2\omega_0 L} (I_0 - I_1) \sin \omega_0 t + \frac{2L - R^2C}{2\omega_0 L^2} (V_0 - V_1) \sin \omega_0 t \right\} \quad (16)$$

Comparing Eqs. (15) and (16), one can conclude that the two switching actions are similar to each other. The magnitude of the undershoots or overshoots is determined by the input and output characteristics of the circuits acting as driver units and as receivers. There is also considerable influence by the capacitance, inductance, and impedance of the connecting cables, including those connections on PC boards, which cannot be neglected at high frequencies.

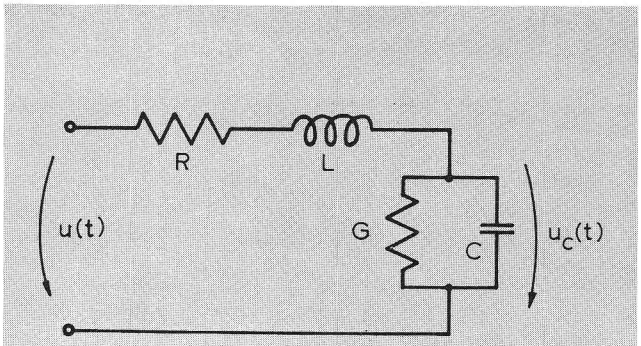

Fig. 1 Circuit schematic of a connection in digital system

Although the analysis on ringing phenomenon in digital systems was carried out based on current switching actions, similar results can be obtained using the voltage equations. Such equations would have the same form; and, as shown in Fig. 2 for the "0" to "1" transition and in Fig. 3 for the "1" to "0", the time diagram would have the two exponential functions $A_1' e\alpha^{1t}$ and $A_2' e\alpha^{2t}$ as limits. An approximation can be made using these equations; the second peak of the ringing has an amplitude which is one-half to one-third of the previous peak (if the first peak is a negative one, then the second is positive; and if the first peak is a positive one, then the second is negative), depending on the impedance of the gates, and the inductance, the capacitance, and the impedance of the connecting cables. Both Figs. 2 and 3 show transient waveforms which can be graphically derived from the voltage equations which have a similar form to Eqs. (15) or (16), using a certain practical value for the impedance, the inductance, and the capacitance involved.

The Voltage Transient in TTL Systems

As can be seen from Eqs. (15) and (16), the main cause of ringing is the reflection of signal transmission through the line. Depending on whether or not the line is terminated properly, this signal will be transmitted back and forth many times.

Because of the high positive threshold level of the TTL gates, the "0" to "1" transition is not as important as the "1" to "0". Also, because TTL ICs have a higher impedance in the off condition than other types, the switching from "0" to "1"—if overswing occurs—will be damped quickly. In practice, one hardly observes such overswing. However, if the line impedance is less than 75 Ω, there is a chance that step transition will occur—and any noise signal can disturb the gate switching during this period. If the line impedance is greater than 150 Ω, positive overshoots can easily be observed.

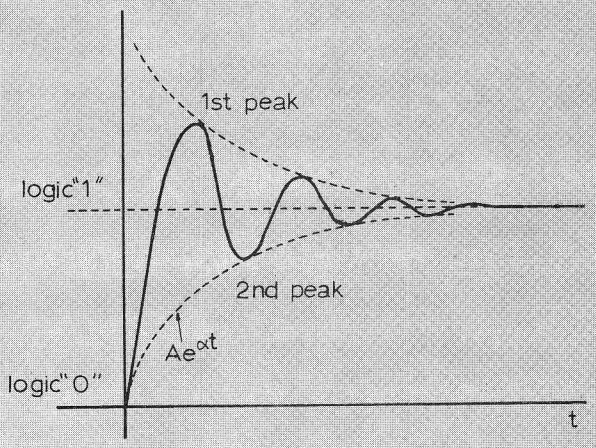

Fig. 2 Voltage transient from logic "0" to logic "1" with ringing

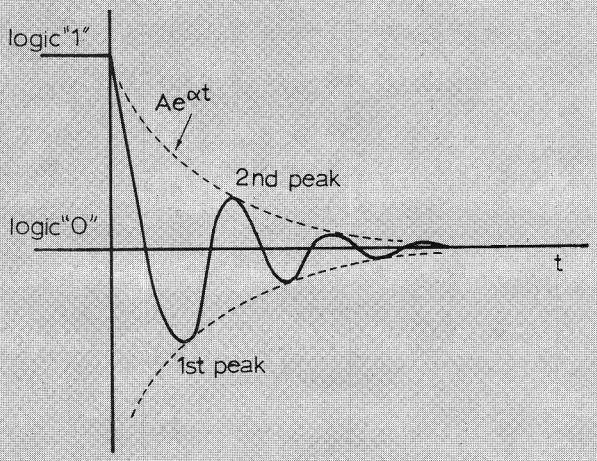

Fig. 3 Voltage transient from logic "1" to logic "0" with ringing

These can damage the devices by providing instantaneous high voltages to the input transistor of the receiving gate and force this gate to break down. Further, if the amplitude of the first negative peak is high enough and exceeds the threshold voltage value of (V_{out} "1" $- V_{in}$"1"), it can cause the receiver gate to switch on a second time, almost immediately after the first trigger edge arrives. This will certainly disturb the system operation and transform the receiving gate from, for example, an inverting unit into a multiply-by-two device. This phenomenon was frequently seen with the previous computer generation when discrete components were used. The ideal solution would be that all connecting cables be terminated with the line characteristic impedance. However, this method is excessively expensive and awkward to realize in practice and is therefore not acceptable to most applications.

The transition "1" to "0" causes other considerations. Fig. 4 shows the reflection diagram of the network indicated in Fig. 5. The connecting cable between the driver gate and the driven one has a characteristic impedance of Z_0. The output characteristics of the driver gate and the input characteristics of the receiver gate are chosen arbitrarily for this discussion. This reflection diagram and the switching time diagram can be directly related to the differential equations as found above. Point A represents the initial voltage level. At this stage, virtually no current is flowing through the connecting cable. The ringing waveform shown is the one which has been transmitted through the line and appears at the input of the driven gate.

Although the first positive peak of this waveform is the main concern, when discussing the ringing phenomenon in digital systems one should not overlook the first negative peak, since this also contributes considerably in the deterioration of the system performance. At the point (B,b), the input under observation can reach a potential of approximately 2.4 V. In normal operating conditions, one or every other input of the receiver gate remains at a high potential; consequently, during a short period, a potential of (V_{in}"h" + 2.4) V will appear between adjacent inputs of the same multiple-emitter transistor. This will cause the input to break down and the gate to stop functioning. During this period—perhaps for a few nanoseconds—excessive current will be drained and the power supply must react correspondingly. This will create noise signals which will be transmitted to other gates and/or logic elements as a result of the crosstalk effect—and thus harmfully disturb them. Cutting down the negative peak to a safe level would not only eliminate this input breakdown effect, but—as discussed above using Eq. (15)—also reduce the positive peak amplitude.

It can be seen clearly from Fig. 4 that both negative and positive peaks can be reduced if the input impedance of the receiving gate becomes smaller and the output impedance of the driver gate greater. To a certain extent, this conclusion is almost independent of the line impedance when kept between 50 and 150 Ω.

Fig. 6 shows the reflection diagram of a typical circuit arrangement consisting of two gates and a connecting cable, which for the purpose of this discussion is assumed to have variable line impedance of 50 to 150 Ω. The input characteristics of the receiver gate can be either normal or clamped.

It is common knowledge that HLTTL ICs have an input threshold of approximately 1.2 V, whereas that of the 7400 series is only 0.8 V. This would mean that

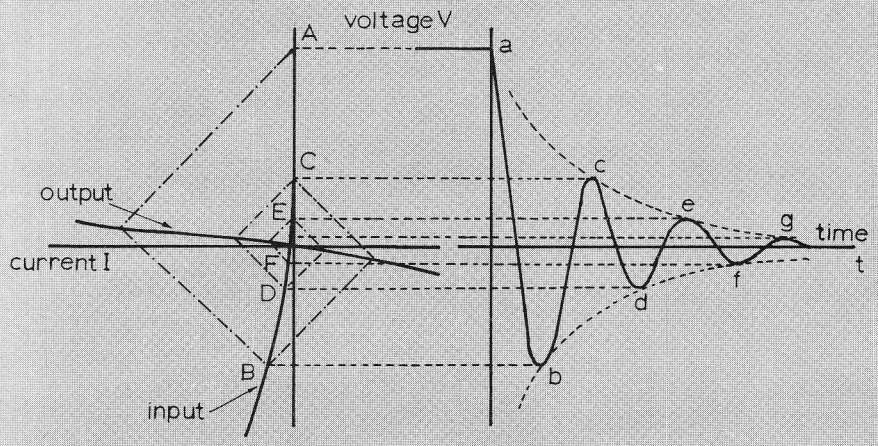

Fig. 4 Graphic analysis of the line reflection

when designing TTL devices using the multiple-function-single-chip approach (also known as the master chip approach) to provide 7400 series devices, a worst case of 0.8 V threshold level must be taken into consideration. If the first positive peak does not exceed this level, the receiving gate will not be disturbed. However, this does not allow any noise protection. Therefore, if efforts can be made to limit the negative peak to a safe level of 0.7 V, the noise protection in a noisy environment for the receiver gate input could be as much as 0.5 to 0.8 V.

With a 150-Ω line impedance, and with the inputs of the driven gate not clamped, the negative peak could be as much as −2.2 V. In this case an increase of the output impedance of the driver gate seems to show no improvement on the ringing. However, if clamping facility is provided, the negative voltage peak can be reduced substantially (point C), and the signal arriving at the input of the receiver gate might not even have a positive overswing. The only trouble which may occur is the possibility of an input breakdown, especially when V_{in}"h" is kept at 4.5 V. In practice, the ringing will be damped because of the reactance of the system connections.

With a line impedance of 100 Ω, and with the inputs not clamped, the negative overshoot is approximately −2.3 V and the positive peak would be 0.5 to 0.6 V. If the output impedance can be controlled, almost no negative peak will be observed. However, if the inputs are clamped (point F), ringing can still occur, but only to a negligible extent. Again in this case input breakdown can be harmful to the system operation. With a 50-Ω line impedance, the negative overswing is quite small and could be regarded as negligible.

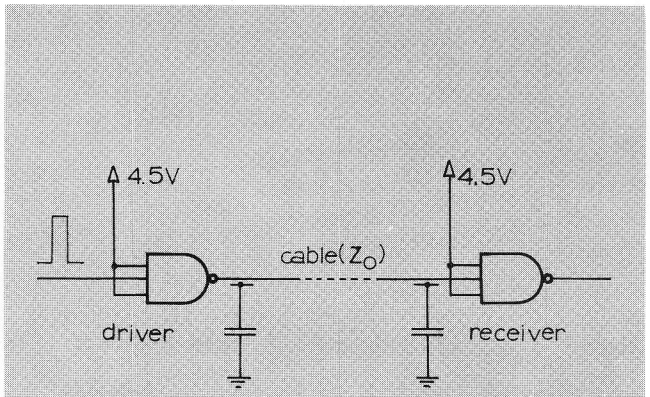

Fig. 5 Circuit arrangement consisting of a driver and a receiver gate

It can be seen from Fig. 6 that input clamping is a necessity. Furthermore, if proper care is taken when designing the output stage of the TTL ICs the ringing effect can be reduced to a minimum. It would be ideal that the input impedance and the output impedance of TTL gates with respect to negative voltage in the system be of the same order as the line impedance. Such a case is, however, impossible to realize and one has to design the ICs to operate satisfactorily in large systems over an impedance range of 50 to 150 Ω.

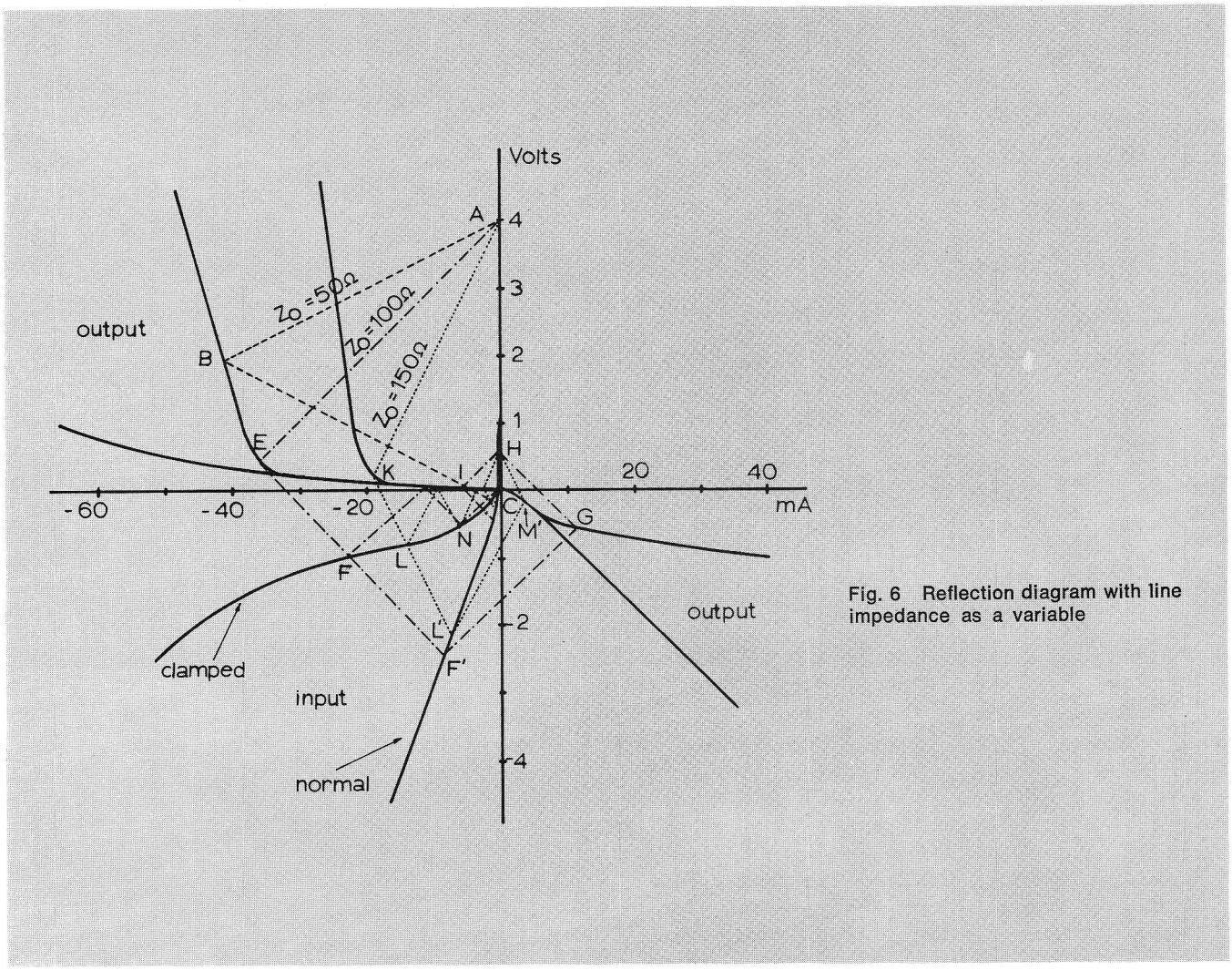

Fig. 6 Reflection diagram with line impedance as a variable

Input Clamping Methods for Digital ICs

There are at least two distinct approaches for providing good immunity to line signal reflection for TTL digital ICs and thus guaranteeing protection against system breakdown due to "illogical" actions of the logic elements.[1] This discussion will only deal with the clamping methods which are feasible at present—conventional and substrate.

Conventional Clamping

This method is the simpler of the two, aiming at the creation of the effect required. A diode is placed at each input of the IC, with its anode connected to the ground level. In order to provide proper matching conditions between driver and driven gates, an effort must also be made to provide output clamping. This means that a 14-lead device could eventually require up to a total of 12 additional diodes. When considering the prospect of good bonding arrangement and of sufficient tolerance limits to achieve improved assembly yield, the extra diodes will cause an increase of the chip (die) dimension by approximately 18 to 20%, compared with a similar layout without the inclusion of the diodes.

In addition, these diodes are active components; thus they are also subject to reliability hazards. Furthermore, the additional interconnections on the chip—between the bonding pad and the appropriate diodes—would mean a lower processing yield and also a deterioration of the system reliability. This is the approach used to provide clamping facility for the 9000 series. Experience of the last few years in the field of processing, especially with respect to the aluminum metal evaporation technique, can, however, guarantee very good metal interconnections; therefore they have helped most manufacturers to overcome such problems as microcrack or others related to the reliability of ICs.

In order to utilize silicon estate to a better degree (and thus eliminate the chip size increase when real clamping diodes are provided), to reduce the chances that the reliability of such devices might be negatively affected due to bad metal connections (between bonding pads and their appropriate diodes), and especially to improve processing yield, some manufacturers have

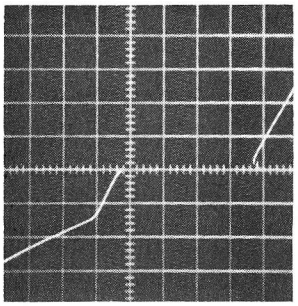

Fig. 7 Input characteristics of a typical TTL gate with substrate clamping (vertical 10 mA/cm, horizontal 2 V/cm)

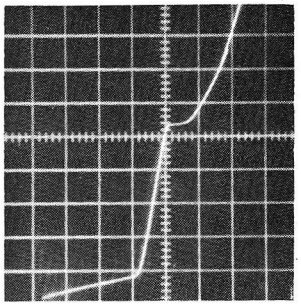

Fig. 8 Output characteristics of a typical TTL gate with substrate clamping (vertical 10 mA/cm, horizontal 2 V/cm)

placed the clamp diodes directly under the bonding pads. This, at first, seems to be quite adequate, at least for the reasons mentioned above. However, another very serious problem has arisen that could easily completely eliminate the clamping effect which the diodes help to provide. These diodes, when placed under the bonding pads, are subject to damage by the bonding pressure, especially when ultrasonic bonding is used. Furthermore, the existence of diffusion profiles under the pads will not guarantee good bonding. It has been proven that such cases have occurred very often and are quite hazardous to the device reliability.

A damaged input diode would certainly not provide the clamping effect required. The main problem for the users of ICs is that such damaged diodes are not easily detected with present testing procedures, especially when clamping is not guaranteed by a test parameter that is agreed to and accepted by both customer and supplier. The presence of such discrete diodes further means an increase in input-to-output delay time of the device, thus making this device unsuitable for high-speed operations. All these problems have led to the utilization of the substrate diode for the purpose of clamping.

Substrate Clamping

This method helps eliminate all the problems previously discussed,[1] by using the parasitic diode provided by the processing diffusions that form the input transistors. The grounded substrate is the anode, and the input transistor collector is the cathode. As can be seen, should the gate input swing to a negative potential, this collector-substrate diode becomes forward-biased and provides a low impedance path for the clamp current to flow through the low-saturated conducting input transistor. This helps drain energy from the line and consequently limits the magnitude of the undershoot to a safe value of approximately 0.7 V.

In order to achieve the desired effect, the total path impedance must be kept as low as possible. The input transistor must be designed to have a low saturation impedance and must only go out of saturation at a current level of 30 to 40 mA. The main measure is, however, the extension of the isolation area by bringing the isolation diffusion out to the edge of the chip (die), so that the total series resistance of the parasitic substrate-to-collector diode is satisfactorily low. This can also be improved by using a low impedance treatment during the diffusion process. One can say that this method is much more advantageous than the discrete clamping approach as described above, especially since this also helps to improve the working speed of the total system built due to a decrease in the delay time of the logic elements used. Furthermore, the nominal capacitance of 3 pF, typically added to each input when discrete on-chip diodes are used, increases the delay considerably, so that improved output stage is normally required. This again increases the total power dissipation of the device and thus limits its applications.

It can be seen then that conventional clamping: reduces the working speed of TTL devices; increases their power dissipation; decreases their reliability with respect to operating performance due to the existence of additional active components (diodes) and on-chip connections (metal paths between the input bonding pads and these diodes); decreases their reliability with respect to bonding and to clamping effect, if these diodes are placed directly under the bonding pads; increases the chip size and thus contributes to a substantial waste of silicon real estate; reduces processing and assembly yield; and does not always provide a matching characteristic between the input of the receiving gate and the output of the driver. Figs. 7 and 8 show input and output characteristics of a typical TTL IC with substrate clamping.

Conclusion

The ringing phenomenon in digital systems built with high-speed ICs, especially with a family such as TTL where fast transients are involved, can be minimized so as to become negligible. TTL ICs with substrate clamping provide good matching characteristics for long line driving, and at the same time offer the possibility of working satisfactorily with line impedance between 30 and 150 Ω. It is worth noticing here that unused inputs are recommended to be tied to the power supply level via a 1-kΩ resistor, so that input breakdown can be avoided and the logic elements used in the system will not react illogically to the command signals.

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